CLAIMS

What is claimed is:

1. An integrated circuit card for a test head, the integrated circuit card comprising:

an I/O channel with an elastomeric connector;

pin electronics integrated circuit (PEIC) coupled to the I/O channel;

micromachine relays coupled to the PEIC;

spring pins coupled to and controlled by the micromachine relays, the spring pins designed to be movably coupled to a device under test (DUT);

a heat sink structure integral to the integrated circuit card to flow a chilled substance through the heat sink structure to cool the PEICs.

2. The integrated circuit card of claim 1, wherein the chilled substance comprises a gas or a liquid.

3. The integrated circuit card of claim 1, wherein the heat sink structure comprises cooling channels within the integrated circuit card.

4. The integrated circuit card of claim 1, wherein the cooling channels are etched, drilled, cast, or micromachined within the integrated circuit card.

5. The integrated circuit card of claim 1, further comprising a driver circuit for driving a movement of the micromachine relay.

6. The integrated circuit card of claim 1, wherein the integrated circuit card further includes a timing generator for generating clocking and timing signals for the PEIC.

7. The integrated circuit card 6, wherein the timing generator is located on the test head, thereby reducing signal delays.

8. The integrated circuit card of claim 1, further comprising a tester for generating the signals used to test the DUT.

9. The integrated circuit card of claim 8, further comprising a logic circuit receiving signals from the tester.

10. The integrated circuit card of claim 9, wherein the logic circuit is located on the test head.

11. The integrated circuit card of claim 9, wherein the logic circuit is a field programmable gate array (FPGA).

12. A testing unit comprising:

a computing system;

a test head coupled to the computing system and receiving control signals from the computing system, the test head having a place for a device under test (DUT), the test head comprising:

a location to place a DUT;

a plurality of spring pins for connecting signals to the DUT;

a plurality of micromachine relays for controlling the plurality of spring pins; and

an integrated circuit device for controlling the relays;

wherein the micromachine relays are included within a substrate of the integrated circuit device.

13. The testing unit of claim 12, wherein the test head is moveable with respect to the computing system.

14. The testing unit of claim 12, wherein the test head is coupled to the computing system via a flexible transmission line.

15. The testing unit of claim 14, wherein the flexible transmission line is a flexible low impedance bus.

16. The testing unit of claim 12, wherein the testing unit further includes a timing generator for generating clocking and timing signals for the integrated circuit device.

17. The testing unit of claim 16, wherein the timing generator is located on the test head, thereby reducing signal delays.

18. The testing unit of claim 12, further comprising a tester for generating the signals used to test the DUT.

19. The testing unit of claim 18, further comprising a logic circuit receiving signals from the tester.

20. The testing unit of claim 12, wherein the test head has a circular body, and the integrated circuit device comprises a plurality of integrated circuit cards located within the test head.

21. The testing unit of claim 20, wherein:
the body of the test head includes a plurality of cut-outs;
the integrated circuit device includes a plurality of circuit cards having tops that fit within the cut-outs of the test head; and
the plurality of spring pins extend from the tops of the circuit cards through the cut-outs.

22. The testing unit of claim 12, further comprising a micromachine relay switch matrix coupled to the integrated circuit device, the micromachine relay switch matrix selectively coupling signals to the plurality of spring pins.

23. The testing unit of claim 22, wherein the micromachine relay switch matrix comprises a plurality of switches implemented on the substrate.

24. The testing unit of claim 22, wherein the micromachine relay switch matrix is implemented on a hybrid circuit.

25. The testing unit of claim 12, wherein the micromachine relay comprises a moveable cantilever arm controlled by electromagnetic attraction/repulsion.

26. The testing unit of claim 12, wherein the micromachine relay comprises rhodium contacts and a ferrite electromagnets.

27. The testing unit of claim 12, wherein the micromachine relay comprises a relay built of micromachined parts.

28. The testing unit of claim 12, wherein the micromachine relay comprises an electrostatic relay.

29. A tester including a moveable test head for testing a device under test (DUT), the test head comprising:

a spring pin array designed to couple the tester to the DUT;

a micromachine relay array designed to control the spring pin array;

an integrated circuit for controlling the micromachine relay array to permit testing of the DUT; and

a control circuitry for controlling a testing of the DUT coupled to the integrated circuit.